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PATENT APPLICATION NO: PI 2000 4237

This is to certify that annexed hereto is a true copy from the records of the Registry of Trade Marks and Patents, Malaysia of the application as originally filed which is identified therein.

authority of the
ISTRAR OF PATENTS

UL RAHMAN RAMLI
ERTIFYING OFFICER)
12 June 2001

KEMENTERI PERDAGANGAN DALAM NEGERI
DAN HAL EHWAL PENGGUNA MALAYSIA
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CERTIFICATE OF FILING

APPLICANT	:	CARSEM SEMICONDUCTOR SDN. BHD.
APPLICATION NO	:	PI 20004237
REQUEST RECEIVED ON	:	13/09/2000
FILING DATE	:	13/09/2000
AGENT'S/APPLICANT'S FILE REF.	:	ISD 426/13/1 [EPD/2000-8/41]

Please find attached, a copy of the Request Form relating to the above application, with the filing date and application number marked thereon in accordance with Regulation 25(1).

Date : 27/09/2000

(HASNON BT. ALANG MOHD RASHID)
for Registrar of Patents

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FF 09

A STRESS-FREE LEAD FRAME

1. Field of the Invention

The present invention relates generally to a lead frame, especially to a stress-free lead frame for semiconductor provided with a stress-relief means and an interlocking means for eliminating delamination of leads during packaging.

2. Background Art of the Invention

The process of manufacturing semiconductor devices involves several steps whereby an integrated circuit chip is bonded to a foil-type lead frame and encapsulated in epoxy or other moulded resin. The lead frame comprises of a plurality of leads etched or stamped out of a thin metallic foil sheet, and the inner ends of the leads are usually bonded to the solder bumps of the integrated circuit chip by a thermal compression method. The chip is then encapsulated in plastic by a transfer moulding process that results in a chip package having the outer ends of the leads expose to the outside for connection to a circuit board.

In a typical prior art system for bonding and encapsulating integrated circuits, a plurality of such circuits is linearly arranged in a single workpiece, which contains a series of identical lead frames etched or stamped on a strip of metallic substrate. A chip is bonded to each of the pre-manufactured lead

frames and they are loaded to a bottom mould with the number of lead frames in a single batch being determined by the mould size and the capacity of the moulding equipment being used. A top mould is moved into place atop the bottom mould and some means is provided within the moulding equipment to heat the moulds to a proper moulding temperature, and to subsequently cool them for curing purposes. The heated moulds are clamped together by the moulding equipment and when the temperature is right, usually at approximately 175°C, the moulding material such as epoxy in pellet form is placed in the mould set through pots formed either in the top or bottom mould. Plungers are then inserted into the pots of the mould and a pressurizing force is applied to the plungers. The combination of the pressurizing force and the heat causes the epoxy pellets to liquify and flow into cavities provided in the mould set, which determines the configuration and the location of the moulded plastic that encapsulate the integrated circuits. Upon completion of this step, the mould set is cooled to induce curing to the epoxy, then the plungers are pulled from the mould set, the mould set is unclamped, and the top mould is lifted from the bottom mould. The lead frames are then removed from the bottom mould and the next station may be trimming, forming, sawing and otherwise operations on them to finish fabrication of the electronic circuit packages. Typically the outer leads of each package need to be bent (formed) to conform to requirements of the printed circuit board for which they are designed.

Delamination, that is separation of the metal lead frame from the moulded epoxy has been reported to happen during handling of the MLP. This is undesirable as it will cause damage and thus render the MLP a reject.

The moulding step also subjects the lead frame to tremendous structural stresses caused by the difference in expansion and compression of the moulded metallic foil that the lead frame and the unmoulded metallic foil that is its outer periphery. This causes bending, waving and twisting of the leads, resulting in delamination of the leads or separation of the metallic lead frame and the epoxy which will results in reliability failure of the package.

Therefore there exists a need for an improved lead frame design that may eliminate delamination problem as mentioned above.

3. Summary of the Invention

Accordingly, it is the primary object of the present invention to provide a stress-free lead frame having a stress-relief and an interlocking means for eliminating delamination of leads during packaging.

It is another object of the present invention to provide a stress-free lead frame having a stress-relief means that can be produced using existing moulding machine.

It is yet another object of the present invention to provide a stress-free lead frame having a stress-relief means that is of simple design for easy production.

These and other object of the present invention is accomplished by,

A stress-free lead frame (1) comprising;

a lead frame (10) having a plurality of integrated circuits (11), each of said plurality of integrated circuits having a die pad (12) and a plurality of leads (13); and

a peripheral pad (14) surrounding said lead frame (10),

characterised by

said peripheral pad (14) being provided with a plurality of stress-relief means (15).

4. Brief description of the drawings

Other aspect of the present invention and their advantages will be discerned after studying the Detailed Description in conjunction with the accompanying drawings in which:

FIG. 1 showing a lead frame of the prior art having a multiple integrated circuit units.

FIG. 2 showing a stress-free lead frame having a stress-relief means according to one embodiment of the present invention.

5. Detailed Description of the Drawings

Referring now to FIG. 1 showing a lead frame of the prior art having a multiple integrated circuit units. A lead frame (2) of the prior art consists of a plurality of integrated circuits (20), each having a die pad (21) and a plurality of leads (22) projecting outwardly from the die pad (21). The integrated

circuits (20) are connected together by connecting bars (23). At the outer periphery of the lead frame (2), there is an inactive portion of the lead frame (2) called a peripheral pad (24). When the lead frame (2) is moulded to form the MLP, about half of the peripheral pad (24) is left unmoulded causing different expansions and thus delamination to the plurality of leads (22) adjacent to the peripheral pad (24).

Referring to FIG. 2 showing a stress-free lead frame having a stress-relief means according to one embodiment of the present invention. The stress-free lead frame (1) comprises a lead frame (10) having a plurality of integrated circuits (11) joined together by connecting bars (12). Each of the integrated circuit (11) is having a plurality of die pads (not shown) and leads (not shown) projecting outwardly from the die pads. A peripheral pad (14) surrounds the lead frame (10).

The lead frame (10) is preferably of a metallic foil base, like copper or other suitable materials. The metallic foil is either etched or stamped to form the lead frame (10) that contain a plurality of integrated circuits (11). Each of the integrated circuit (11) has a die pad (not shown) for attaching a die and a plurality of leads (not shown) projecting away from the die pads. The lead frame (10) is surrounded by a peripheral pad (14) that is an inactive part of the metallic foil. The peripheral pad (14) is provided with a plurality of stress-relief means (15) and a plurality of interlocking means (16)

in the form of holes and slots. Extensive research and experimentation has revealed that for best result, at least three rows of stress-relief means (15), a first row, a second row and a third row, and a row of interlocking means (16) are needed. The first and the third row of the stress-relief means (15) are provided with slots while the second row is provided with holes, preferably square hole. The holes and slots are arranged side by side in equal intervals for equal expansion and compression distribution. For the interlocking means (16), a plurality of slots are arranged at equal intervals in between the second and the third row of the stress-relief means (15).

During moulding, the lead frame (10) and the peripheral pad (14) containing the stress-relief means (15) and the interlocking means (16) is moulded to form the MLP. The heat produced during this process causes the leads to expand and to compress when cooled. In prior art practice, this produces delamination that causes many of the resulting integrated circuits a reject. However, the provision of the stress-relief means (15) can easily accommodate the expansion and compression of the leads. Further, the interlocking means (16) holds firmly the lead frame (10) to the moulded epoxy thus eliminating altogether delamination in the leads caused either by expansion and contraction of the metal lead frame or during handling of the MLP.

While the preferred embodiment of the present invention and their advantages have been disclosed in the above Detailed Description, the invention is not

limited thereto but only by the spirit and scope of the appended claim.

What is claimed is:

1. A stress-free lead frame (1) comprising;

a lead frame (10) having a plurality of integrated circuits (11), each of said plurality of integrated circuits having a die pad (12) and a plurality of leads (13); and

a peripheral pad (14) surrounding said lead frame (10),

characterised by

said peripheral pad (14) being provided with a plurality of stress-relief means (15).

2. A stress-free lead frame (1) comprising;

a lead frame (10) having a plurality of integrated circuits (11), each of said plurality of integrated circuits having a die pad (12) and a plurality of leads (13); and

a peripheral pad (14) surrounding said lead frame (10),

characterised by

said peripheral pad (14) being provided with a plurality of interlocking means (16).

3. A stress-free lead frame (1) as claimed in Claim 1 further characterised by said plurality of stress-relief means (12) being holes and slots.

4. A stress-free lead frame (2) as claimed in Claim 1 further characterised by said holes and slots being arranged in multiple rows.

5. A stress-free lead frame (3) as claimed in Claim 2 further characterised by said interlocking means (16) being a plurality of slots.

6. A stress-free lead frame (1) as claimed in Claim 4 or Claim 5 further characterised by said holes and slots are arranged side by side at equal intervals.

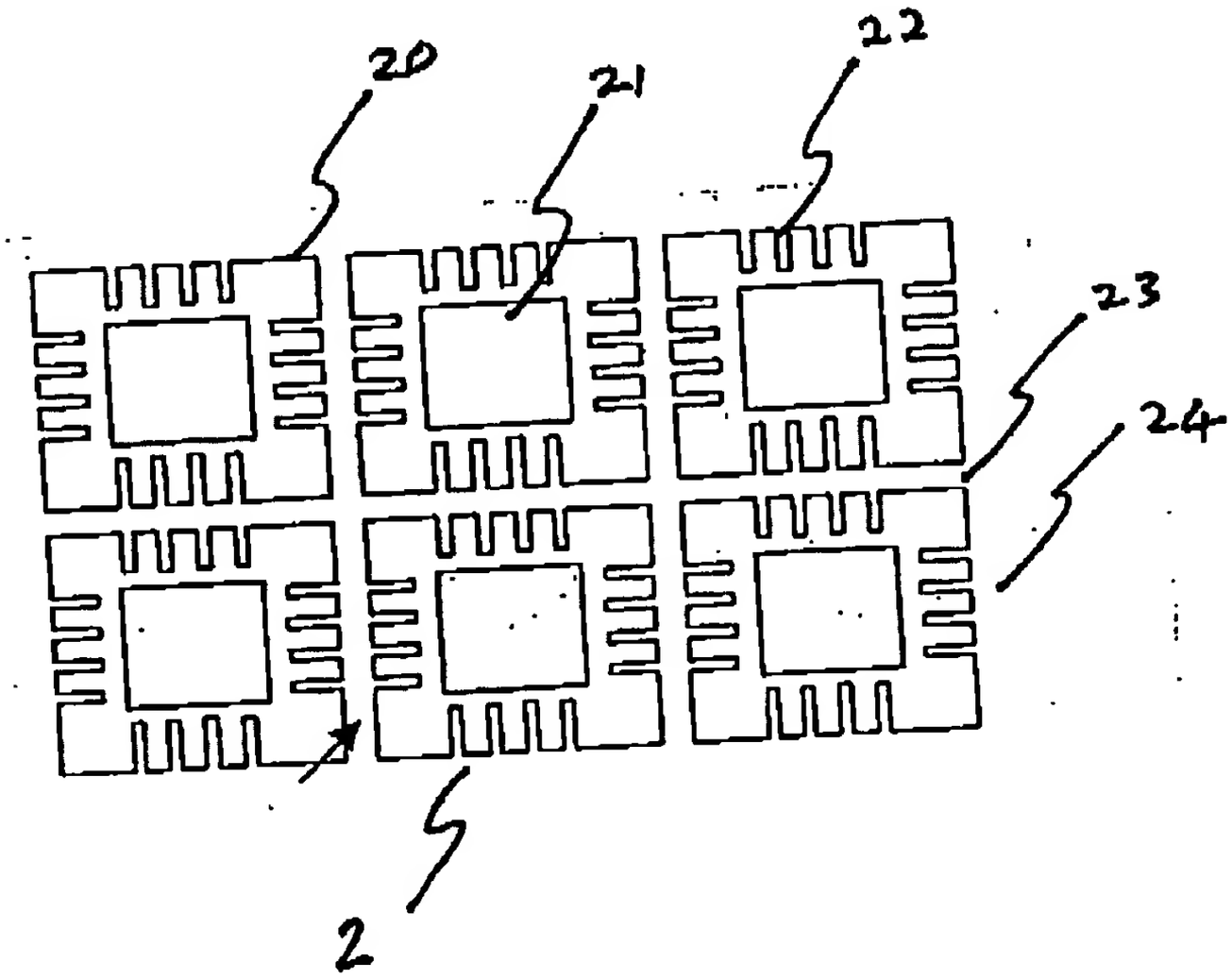

FIG. 1

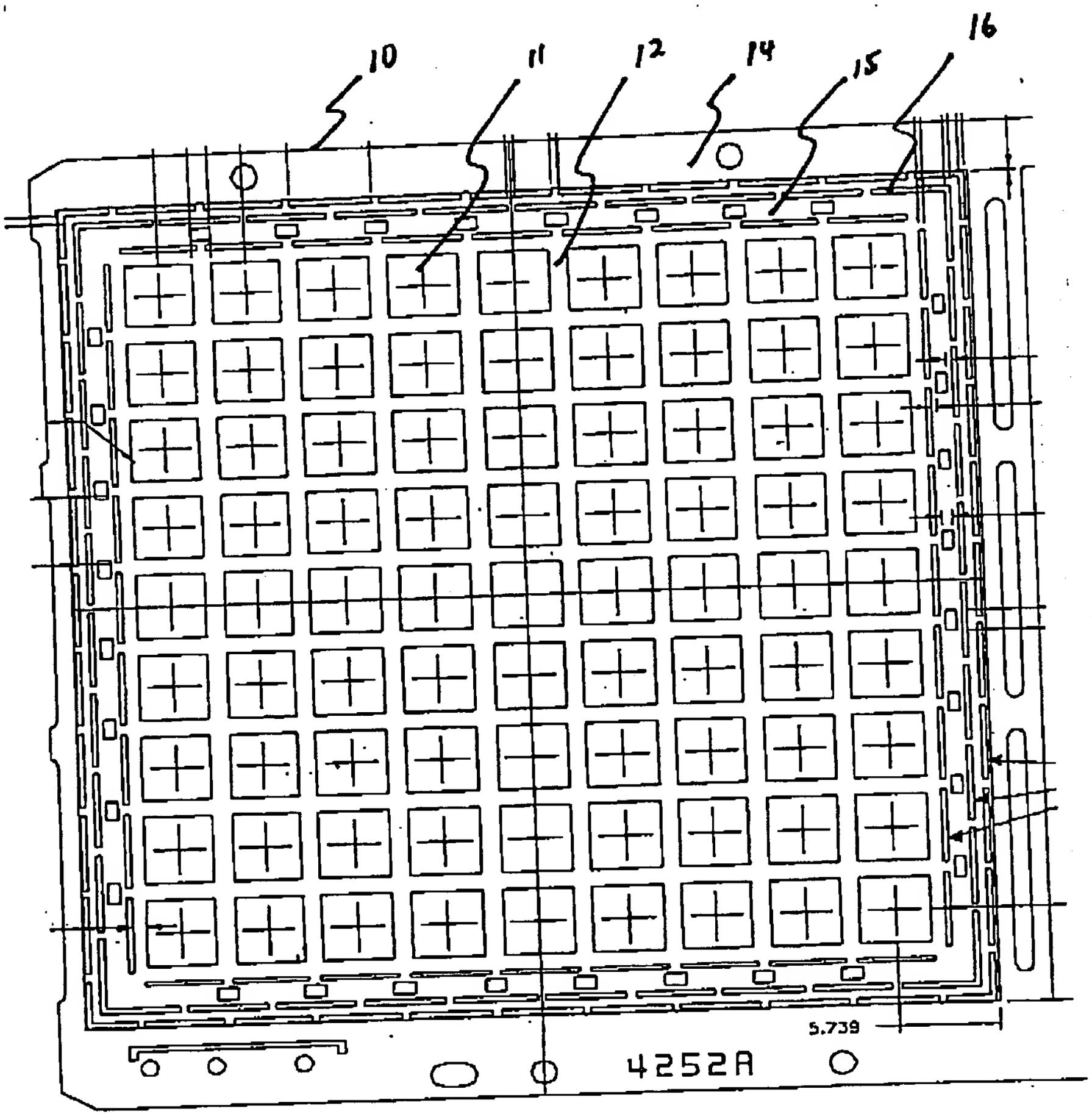

FIG. 2

ABSTRACT

A STRESS-FREE LEAD FRAME

The present invention relates to a stress-free lead frame (1) for a semiconductor. The stress-free lead frame (1) is provided with a stress-relief means (15) and an interlocking means (16) at the outer periphery. The stress-relief means (15) is capable of accommodating expansion and compression while the interlocking means (16) take care of shock and vibration during handling to thereby eliminate delamination of the lead frame (10).

(The most illustrative drawing is FIG. 3)

Patents F rm No. 1
PATENTS ACT 1983

REQUEST FOR GRANT OF PATENT
[Regulations 7(1)]

To : The Registrar of Patents
Patent Registration Office
Kuala Lumpur,
Malaysia

For Official Use

APPLICATION RECEIVED NO. : PI 20004237

Fee received on: 13-9-2000

Amount : RM 960.00

*Cheque/Postal Order/Money Order/Draft/Cash

Bank Cek

Date of mailing :

Please submit this Form in duplicate
Together with the prescribed fee.

Applicant's Reference :

ISD 426/13/1 [EPD/2000-8/41]

THE APPLICANT(S) REQUEST(S) THE GRANT OF A PATENT IN RESPECT OF THE FOLLOWING PARTICULARS

I. TITLE OF INVENTION : A STRESS-FREE LEAD FRAME

II. APPLICANT(s) the data concerning each applicant must appear in this box or, if the space is insufficient, in the space below)

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Telephone Number
(if any)

03-5446131

Fax Number
(if any)

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13 SEP 2000
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Bahagian

Additional Information (if any)

20004237

VI. DISCL Addit

III. INVENTOR

Applicant is the inventor Yes ☐ No ☑

If the applicant is not the inventor :

Name of inventor : As attached

Address of inventor : As attached

A statement justifying the applicant's right to the patent accompanies this Form :

Yes ☑ No ☐

Additional Information (if any)

IV. AGENT OR REPRESENTATIVE

Applicant has appointed a patent agent in accompanying Form No. 17

Yes ☑

No ☐

Agent's Registration No. : PA/2000/0104

Applicants have appointed Sahani Ahmad
To be their common representative

V. DIVISIONAL APPLICATION

This application is a divisional application ☐

The benefit of the

filing date priority date ☐

of the initial application is claimed in as much as the subject-matter of the present application is contained in the initial application identified below :

Initial Application No. :

Date of filing of initial application :

VI. DISCLOSURE TO BE DISREGARDED FOR PRIOR ART PURPOSES

Additional information is contained in supplemental box : ☐

(a) Disclosure was due to acts of applicant or his predecessor in title ☐

Date of disclosure: _____

(b) Disclosure was due to abuse of rights of applicant or his predecessor in title ☐

Date of disclosure: _____

A statement specifying in more detail the facts concerning the disclosure accompanies this Form

Yes ☐

No ☐

Additional Information (If any)

VII. PRIORITY CLAIM (if any)

The priority of an earlier application is claimed as follows :

Country (if the earlier application is a regional or international application, indicate the office with Which it is filed) : _____

Filing Date : _____

Application No. : _____

Symbol of the International Patent Classification :

If not yet allocated, please tick ☐

The priority of more than one earlier application is claimed:

Yes ☐ No ☐

The certified copy of the earlier application(s) accompanies this Form:

Yes ☐ No ☐

If No, it will be furnished by

Additional Information (if any)

DITERIMA
13 SEP 2000
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Bahagian
Harta Intelek

20004237

VIII. CHECK LIST

A. This application contains the following :

1. request		Sheets
2. description	7	Sheets
3. claim	2	Sheets
4. abstract	1	Sheets
5. drawings	2	Sheets
Total	12	Sheets

B. This Form, as filed, is accompanied by the items checked below :

(a) signed Form No. 17	✓
(b) declaration that inventor does not wish to be named in the patent assignment	
(c) statement justifying applicant's right to the patent	✓
(e) priority document (certified copy of earlier application)	
(f) ~~cash~~, cheque, ~~money order~~, banker's draft ~~or postal order~~ for the payment of application fee	✓
(g) other documents (specify) – Form 5	✓

IX. SIGNATURE _____ 13/9/2006

Sahrani Ahmad
**(Applicant/Agent) (Date)

If Agent, indicate Agent's Registration No. : PA/2000/0104

For Official Use

1. Date application received :

2. Date of receipt of correction, later filed papers or drawings completing the application :

* Delete whichever does not apply
** Type nam under signature and delete whichever does not apply

PNMB., K.L.

Sheets

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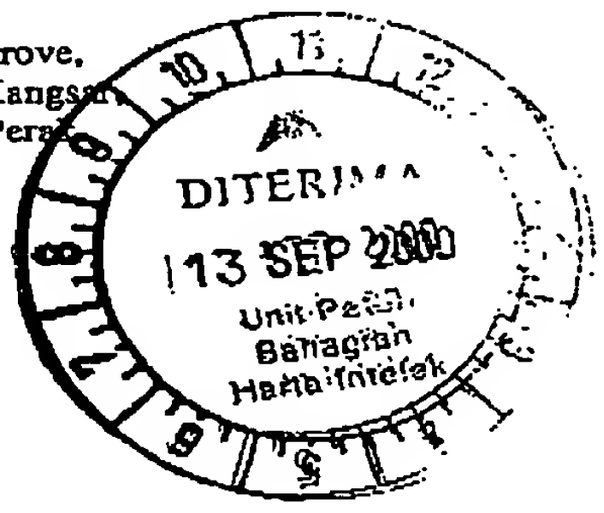

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